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Effects of fin geometry on boiling heat transfer from silicon chips with micro-pin-fins immersed in FC-72

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Abstract

Experiments were performed to study the effects of the height and thickness of square micro-pin-fin on boiling heat transfer from silicon chips immersed in a pool of degassed or gas-dissolved FC-72. Six kinds of micro-pin-fins with the dimensions of 30×60, 30×120, 30×200, 50×60, 50×200 and 50×270 μm^2 (thickness, $t\times$height, h) were fabricated on the surface of a square silicon chip with the dimensions of $10\times10\times0.5$ mm^3 by using the dry etching technique. The fin pitch was twice the fin thickness. The experiments were conducted at the liquid subcooling, ΔT_{sub}, of 0, 3, 25 and 45 K under the atmospheric condition. The results were compared with previous results for a smooth chip and three chips with enhanced heat transfer surfaces. The micro-pin-finned chips showed a considerable heat transfer enhancement in the nucleate boiling region and increase in the critical heat flux, q_{CHF}, as compared to the smooth chip. The wall temperature at the CHF point was always less than the maximum allowable temperature for LSI chips ($=85$ °C). For a fixed value of t, q_{CHF} increased monotonically with increasing h. The increase was more significant for larger t. The q_{CHF} increased almost linearly with increasing ΔT_{sub}. The maximum value of allowable heat flux ($=84.5$ W/cm^2), 4.2 times as large as that for the smooth chip, was obtained by the chip with $h = 270$ μm and $t = 50$ μm at $\Delta T_{sub} = 45$ K.

Keywords: Boiling; Devices; Heat transfer enhancement; Finned surfaces; FC-72

1. Introduction

Direct liquid cooling, involving boiling heat transfer, by use of dielectric liquids has been considered as one of the promising cooling schemes for high-powered electronic devices. For most memory and logic chips, a sophisticated cooling technology is needed to maintain a relatively constant component temperature below 85 °C. Thus, primary issues related to the direct liquid cooling are the mitigation of temperature overshoot at boiling incipience, enhancement of nucleate boiling and increasing the critical heat flux.

Many studies have dealt with the enhancement of boiling heat transfer from electronic devices by use of surface microstructures that were fabricated directly on a silicon chip. These include a sand-blasted and KOH treated surface [1], a dendritic heat sink (a brush-like structure) [1,2], laser-drilled holes (3–15 μm in mouth dia.) [3], re-entrant cavities (0.23–0.5 mm in mouth dia.) [4], alumina particle (0.3–5 μm in dia.) spraying and painting of diamond particles (1–12 μm in dia.) [5], micro-re-entrant cavities (1–3 μm in mouth dia.) [6], a submicron-scale roughness produced by sputtering of SiO_2 film and then wet etching of the surface (about 30 nm in r.m.s. roughness) [7] and micro-pin-fins produced by dry etching (10–50 μm in thickness and 60 μm in height) [7,8]. The second group, in which the surface structures were fabricated on a simulated chip, includes alumina particle (0.3–3 μm in dia.) spraying [9] and

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Nomenclature

A	projected surface area of chip (cm^2)
A_t	surface area of top surface (cm^2)
h	fin height (μm)
p	fin pitch (μm)
q	heat flux based on projected surface area (W/cm^2)
q_{CHF}	critical heat flux (W/cm^2)
$q_{CHF,S}$	critical heat flux of smooth surface (W/cm^2)
q_{max}	maximum allowable heat flux (W/cm^2)
T_b	temperature of bulk liquid (°C)
T_{sat}	saturation temperature (°C)
T_w	reference wall temperature (°C)
$T_{w,CHF}$	wall temperature at CHF point (°C)
$T_{w,i}$	wall temperature at boiling incipience (°C)
ΔT_{sat}	wall superheat $= T_w - T_{sat}$ (K)
$\Delta T_{sat,i}$	wall superheat at boiling incipience $= T_{w,i} - T_{sat}$ (K)
ΔT_{sub}	liquid subcooling $= T_{sat} - T_b$ (K)
t	fin thickness (μm)
y_g	mole fraction of dissolved air (–)

Greek symbol

τ	time (ms)

painting of diamond particles (1–12 μm in dia.) [5], silver flakes (3–10 μm in thickness) [10], and aluminum and copper particles [11]. Heat sink studs with drilled holes, micro-fins with and without microporous coating, micro-channels and pores, etc. (0.2–12 mm in feature size) [12–18] have also been tested. While most of the experiments were conducted for saturated condition, a number of studies have dealt with the effects of liquid subcooling [7,8,14,19] and dissolved gas content in the liquid [7,8,20].

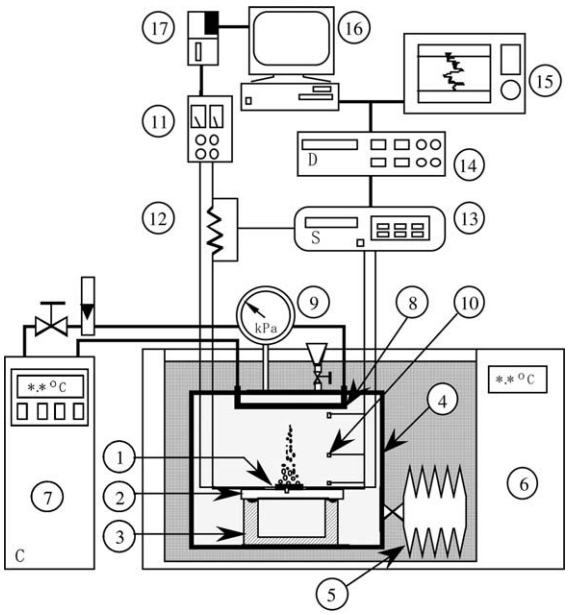
Recently, Honda et al. [7] studied the effects of square micro-pin-fins (50×60 μm^2 in thickness × height and 100 μm in fin pitch) and submicron-scale roughness (about 30 nm in r.m.s. roughness) on boiling of FC-72 (dielectric fluorocarbon liquid with the saturation temperature $T_{sat} = 56$ °C at normal boiling point). The micro-pin-finned chips showed a sharp increase in the heat flux with increasing wall superheat in the nucleate boiling region and the wall temperature at the CHF point was lower than 85 °C. The micro-pin-finned chip with submicron-scale roughness showed a higher heat transfer performance in the nucleate boiling region and the critical heat flux, q_{CHF}, was 1.8–2.3 times as large as that for a smooth. Honda et al. [8] further studied the effect of the thickness of square micro-pin-fin on boiling of FC-72. The fin dimensions were 10×60, 20×60, 30×60 and 50×60 μm^2 (thickness × height) and the fin pitch was twice the fin thickness. The size of micro-pin-fin that showed the highest critical heat flux decreased with increasing liquid subcooling. The highest critical heat flux obtained by these chips was close to that obtained by the micro-pin-finned chip with submicron-scale roughness on it [7].

The objective of this paper is to study the combined effects of fin thickness and fin height on the boiling heat transfer from silicon chips immersed in degassed and gas-disssolved FC-72. Following the previous results [8], six kinds of micro-pin-finned chips with the fin thickness of 30 and 50 μm and the fin height of 60–270 μm were tested. The results are compared with those for a smooth chip (chip S) and previously reported results for three chips with enhanced surfaces [1,14,19].

2. Experimental apparatus and procedure

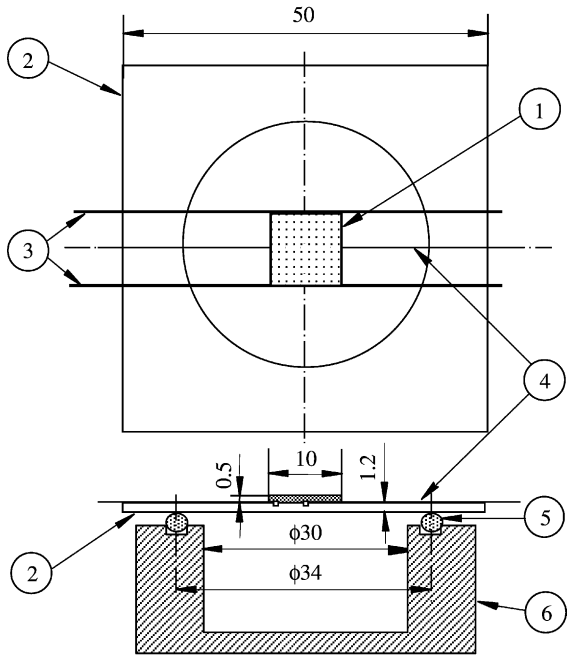
The test facility is shown schematically in Fig. 1. FC-72 was contained within a rectangular test vessel made of stainless steel that was submerged in a temperature-controlled water bath. The test vessel was fitted with viewing windows. The bulk temperature of FC-72 within the test vessel was maintained at a prescribed value by controlling the water temperature inside the water bath. In order to maintain a nearly atmospheric pressure in the test vessel, a rubber bag was attached to it. A test section consisting of a test chip bonded on a pyrex glass plate and fixed on a vacuum chuck made of brass was immersed horizontally in the test vessel.

Details of the test section are shown in Fig. 2. The test chip was a P doped N-type silicon chip with the dimensions of $10\times10\times0.5$ mm^3. The test chip was bonded on a Pyrex glass plate using epoxy adhesive. It was cured in an oven maintained at 373 K with a weight resting on the chip. The vacuum chuck was designed to hold the glass plate by suction and to minimize heat loss due to heat conduction through the glass plate. The side surfaces of the chip were covered with adhesive to minimize heat loss. Therefore, only the upper surface of the chip was effective for heat transfer. For the enhancement of boiling heat transfer, micro-pin-fins with square cross-sections were fabricated on the surface of silicon chip by use of the dry etching technique. To study the combined effects of fin thickness, t, and fin height, h, six kinds of micro-pin-finned chips with the fin dimensions of 30×60, 30×120, 30×200, 50×60, 50×200 and 50×270 μm^2 ($t \times h$), named chips PF30-60, PF30-120, PF30-200, PF50-60, PF50-200 and PF50-270, respectively, were fabricated. The fin pitch p was twice the fin thickness for all chips.



1. Test chip
2. Glass plate
3. Vacuum chuck
4. Test vessel
5. Rubber bag
6. Water bath
7. Cooling unit
8. Condenser
9. Pressure gauge
10. Thermocouples
11. DC power supply
12. Standard resistor
13. Scanner
14. Digital multimeter
15. Pen recorder
16. Computer
17. Power supply controller

Fig. 1. Schematic diagram of experimental apparatus.



1. Silicon chip
2. Pyrex glass plate
3. Copper lead wire
4. Thermocouple
5. O-ring
6. Vacuum chuck

Fig. 2. Details of test section.

The scanning-electron-micrograph (SEM) images of chips PF50-60, PF50-200 and PF50-270 are shown in Fig. 3(a), (b) and (c), respectively. The lower column of each figure shows the close-up of micro-pin-fin. As seen from these figures, the top surface of fin is very smooth. However, a fine roughness is observed on the fin flank. The roughness scale depends on the dry etching condition and it increases in the order of chips PF50-60, PF50-270 and PF50-200.

The chip was Joule heated by using a programmable d.c. power supply. The power supply was connected in series to a standard resistor (1 Ω) and the test chip. The standard resistor was used to measure the electric current in the circuit. In order to prevent real heater burnout, an overheating protection system was incorporated in the power circuit. Two 0.25-mm diameter copper wires for power supply and voltage drop measurement were soldered with a low temperature solder (melting point of 180 °C) to the side surfaces of the chip at the opposite ends. In order to secure the ohmic contact between the test chip and the copper wire, a special solder with the melting point of 300 °C was applied to the chip before soldering the copper wire. Two 0.12-mm diameter T-type thermocouples for the local wall temperature measurement were bonded on the bottom surface of test chip at the center and at about 1.5 mm from the edge using epoxy adhesive. The local temperatures of test liquid at the chip level, and 40 and 80 mm above the chip level were measured by T-type thermocouples that were arranged on a vertical line 25 mm apart from the edge of the test chip. The thermocouples for the measurements of liquid and wall temperatures were calibrated by using temperature controlled water and oil baths. The bath temperature was measured by a platinum resistance thermometer with an accuracy of 0.03 K. The e.m.f.s of the thermocouples were read and recorded consecutively eight times by a data logger to 1 μV and the average values of the eight measurements were adopted as the experimental data. The average chip temperature was also measured by the resistance thermometry. In order to obtain a calibration curve between the temperature and electric resistance of the test chip, the test chip was immersed in a bath of FC-40 ($T_{sat} = 150$ °C at atmospheric pressure) that was immersed in a temperature-controlled oil bath and a constant current of about 1 mA was passed through the circuit. The bath temperature was measured by the platinum resistance thermometer and the voltage drops of the test chip (of the order of 50 mV) and the standard

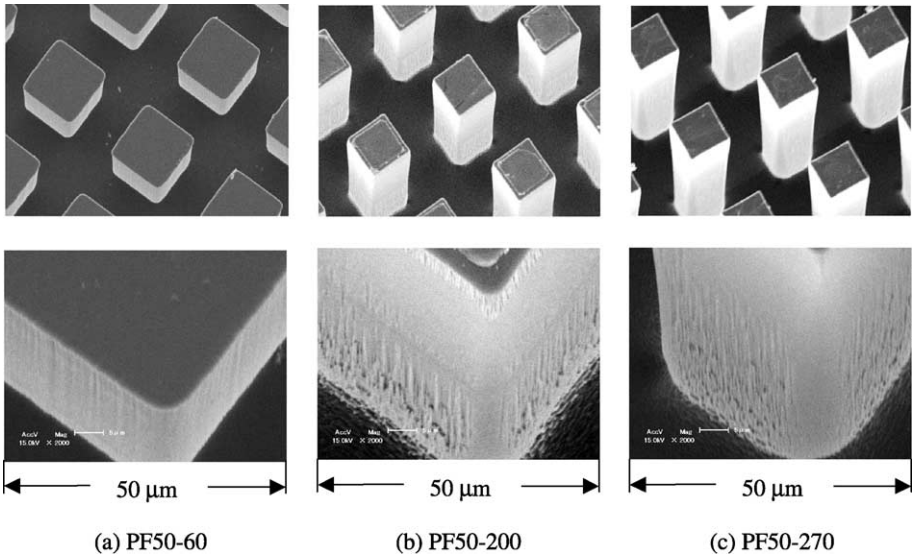


Fig. 3. SEM view of silicon chips with micro-pin-fins.

resistor (about 1 mV) were measured by the data logger in the same manner as the case of the thermocouples. The measured electric resistance of the test chip ranged from 38 to 56 Ω at 60 °C depending on the fin height. The sensitivity of the resistance thermometry was about 0.24 mV/K, which was much higher than that of the T-type thermocouple (about 0.043 mV/K).

Experiments were conducted at the liquid subcooling, ΔT_{sub}, of 0, 3, 25 and 45 K. Prior to the experiments, the test fluid was degassed by maintaining the water temperature inside the water bath at about 63 °C for 4 h while operating the downward facing condenser located at the ceiling of the test vessel. For the cases of $\Delta T_{sub} =$ 25 and 45 K, experiments were also conducted with a gas-dissolved FC-72. In these cases a pressurized air was bubbled into the test liquid for about 12 h and then the test liquid was exposed to ambient air for 12 h. The mole fraction of dissolved air, y_g, was measured by a gas chromatograph. The measured value of y_g was about 2.1×10^{-4}–3.4×10^{-4} and 2.6×10^{-3}–3.3×10^{-3} for the degassed and gas-dissolved FC-72, respectively. The value of y_g before and after a series of experiments were almost unchanged.

Power input to the test chip was increased in small steps up to the high heat flux region of nucleate boiling. The wall temperature of test chip and the bulk liquid temperature were monitored by a pen recorder. The highest value of wall temperature just before the boiling incipience was read from the chart of the pen recorder. After each increase in the power input, about 5 min was imposed to reach a steady state. Then e.m.f.s of the thermocouples and the voltage drops of the test chip and the standard resistor were read and recorded eight times using a data logger to 1 μV and the average values of measurements were adopted as the experimental data. The heat flux, q, (defined on the projected area basis) was obtained from the voltage drop of test chip and the electric current. For the value of q greater than 95 percent of q_{CHF}, the increment of electric current was reduced to a value that corresponded to the increment of q of 0.5 W/cm^2 or less. If the increase of wall temperature greater than 30 K was detected, the data acquisition algorithm assumed the occurrence of the critical-heat-flux (CHF) condition and immediately shut down the power supply. The steady state heat flux value just prior to the shut down was adopted as q_{CHF}. The uncertainties in the chip and bulk liquid temperature measurements by the thermocouple and the resistance thermometry are estimated to be less than 0.1 K. The uncertainty in the calculated value of q is mostly due to the heat loss and estimated to be less than 15 and 5.0 percents for natural convection and nucleate boiling regions, respectively. It should be mentioned that q includes the heat transferred to the bulk liquid by conduction through the copper lead wires and the glass substrate.

The definition of reference wall temperature is an important problem for the microstructured surfaces. For the pin-finned surface, it is possible to estimate the distribution of temperature along the fin based on the assumption of uniform heat transfer coefficient. However, for the dendritic and porous surfaces, it is impossible to estimate the temperature distribution. For both cases, boiling occurs mainly within the surface microstructure where the wall temperature changes considerably. Thus there is no definite guiding principle to define the reference wall temperature. Since these studies are application oriented, and the most important restriction in the electronic cooling is the maximum allowable tem-

perature for LSI chips, an appropriate definition of the reference wall temperature would be the temperature at fin root or the temperature at the top of heating element on which the porous layer is formed.

Generally, the measured wall temperature at the center of chip was higher than that near the edge. The difference increased with increasing q, reaching 6.5 K at the highest q ($=85$ W/cm^2). In the data reduction, the reference wall temperature, T_w, of the micro-pin-finned chip was defined by the temperature at the fin root at the center of chip. The T_w was obtained from the measured temperature at the center of chip on the bottom surface making a small correction (less than 1 K) for wall conduction. A uniform heat generation in the chip and adiabatic condition at the bottom surface was assumed in the calculation. The bulk temperature of test liquid, T_b, was defined by the measured value at the chip level.

The experiment was repeated three times for all chips. The time interval between the subsequent runs was greater than 0.5 h. The boiling curves showed a good repeatability for all cases except for the boiling incipience point. Thus, only the results for the third runs are presented in the next section. Most of the experiments were conducted at the horizontal upward orientation of the chip. Additional experiments with vertically mounted chips were conducted to take video pictures of the boiling phenomena.

3. Experimental results and discussion

Fig. 4(a)–(c) show photographs of local boiling phenomena of gas-dissolved FC-72 at $\Delta T_{sub} = 25$ K on the vertically mounted chip PF50-200. The positions on the boiling curve corresponding to these figures are shown in Fig. 7. Fig. 4(a) corresponds to the boiling incipience point where several nucleation sites appear on the chip surface. The bubbles emerge from the gap between adjacent fins and move upward sliding the chip surface. The vapor bubbles grow as they move upward due to the absorption of vapor supplied by the evaporation of superheated liquid on the chip surface. Fig. 4(b) corresponds to the medium-heat-flux region of nucleate boiling. The distribution of bubbles on the surface is almost uniform. Small bubbles merge with the other adjacent bubbles to form larger ones. Thus the range of bubble size becomes wider. The image of fin pattern just below a large bubble is distorted. This is due to the refraction of light caused by the liquid density variation near the rising bubble. It is also seen that not all of the small bubbles show a clear profile. This indicates that a number of small bubbles are still held within the gap between adjacent fins. Fig. 4(c) shows the lower part of the chip surface at a point just below the CHF point. Small bubbles generated on the chip surface merge into a very large secondary bubble that covers most of the chip surface. The secondary bubble rises along the chip continuously absorbing the newly generated small bubbles. Then the secondary bubble leaves the chip and the next cycle of bubble growth starts.

Fig. 5 shows the sequence of boiling phenomena of gas-dissolved FC-72 on the vertically mounted chip PF50-200 at $\Delta T_{sub} = 25$ K, $\Delta T_{sat} = 9.6$ K and $q = 6.2$ W/cm^2 that corresponds to point (d) in Fig. 7. The arrow in each figure indicates one of the sites where bubble nucleation occurs. At time $\tau = 0$ ms, a bubble leaves the site on the surface. The bubble moves upward thereby increasing its volume. At $\tau = 9$ ms, a small bubble emerges from the gap between adjacent fins. The bubble continues to grow on the surface moving slowly upward. At $\tau = 18$ ms, the bubble detaches the site and the next cycle of bubble growth starts. The average period of bubble emission from the site was about 23.0 ms.

Fig. 6 shows the results for chip S at $\Delta T_{sub} = 25$ K, $\Delta T_{sat} = 9.2$ K and $q = 6.0$ W/cm^2 that corresponds to point (e) in Fig. 7. At time $\tau = 0$ ms, a tiny bubble is left on the surface as a large bubble moves upward. The small bubble continues to grow on the surface. At $\tau = 6$ ms, the

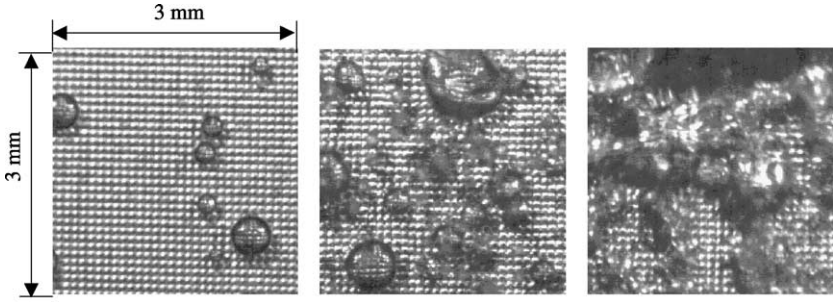


Fig. 4. Photographs of boiling phenomena on vertically mounted chip PF50-200; $\Delta T_{sub} = 25$ K, gas dissolved.

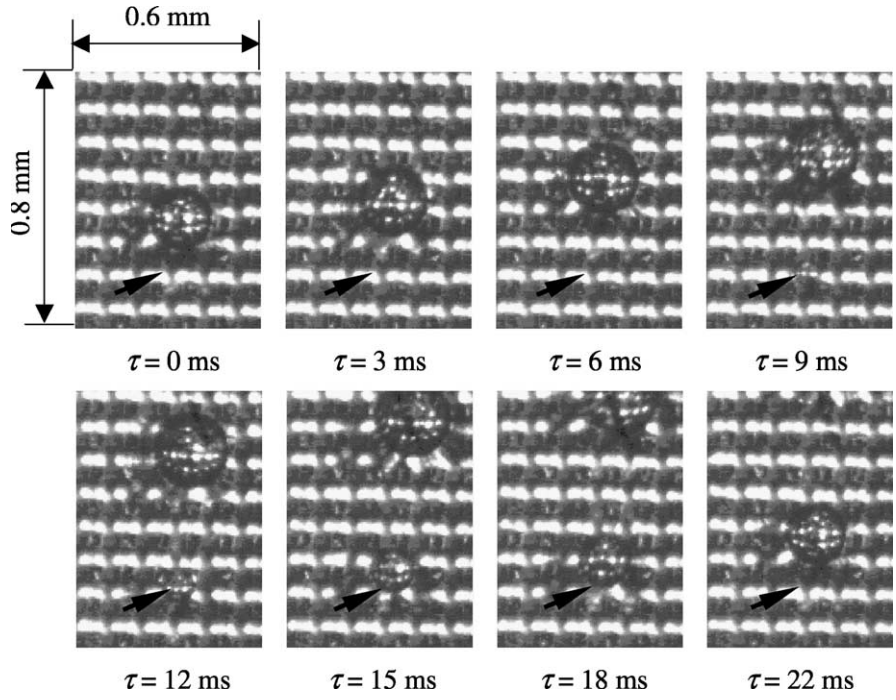


Fig. 5. Behavior of growing bubble on chip PF50-200; $\Delta T_{sub} = 25$ K, gas-dissolved, $\Delta T_{sat} = 9.6$ K and $q = 6.2$ W/cm^2.

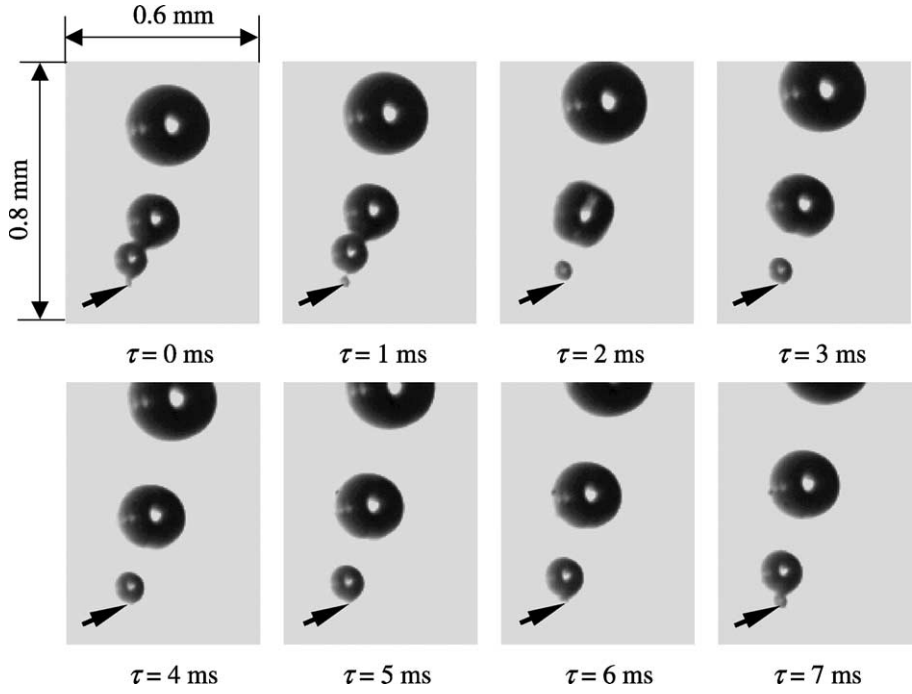


Fig. 6. Behavior of growing bubble on chip S; $\Delta T_{sub} = 25$ K, gas-dissolved, $\Delta T_{sat} = 9.2$ K and $q = 6.0$ W/cm^2.

bubble begins to move upward, thereby leaving a tiny bubble on the surface. Then the next cycle of bubble growth starts. The average period of bubble emission from the site was 5.7 ms. This value is much shorter than

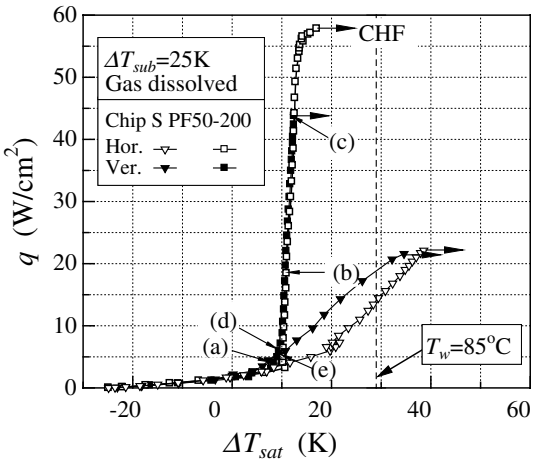


Fig. 7. Comparison of boiling curves for horizontally mounted and vertically mounted chips S and PF50-200; $\Delta T_{sub} = 25$ K, gas-dissolved.

the above-mentioned value for chip PF50-200. It is relevant to note here that the average period of bubble emission for chip PF50-60 with smaller h than chip PF50-200 was about 17.7 ms at $\Delta T_{sub} = 25$ K, $\Delta T_{sat} = 9.8$ K and $q = 6.4$ W/cm^2. Thus the micro-pin-fins act to hold the growing bubbles within the gap between adjacent fins. For bubbles with similar size, the period of bubble emission is longer for higher fin.

It should be mentioned here that the behavior of growing bubble shown in Figs. 5 and 6 are for the low-heat-flux region where free convection effect is dominant. Thus the heat transfer characteristics are little affected by the behavior of growing bubble (see Fig. 7). However, in the fully developed nucleate boiling region where the heat transfer characteristics are dominated by the bubble growth on the chip surface, the above difference in the bubble behavior is supposed to play an important role.

Fig. 7 compares the boiling curves of horizontally mounted and vertically mounted chips S and PF50-200. For chip PF50-200, the value of q in the low-heat-flux region is somewhat higher for the vertically mounted chip but the boiling curve in the fully developed nucleate boiling region is close to each other. Thus the boiling phenomena are little affected by the direction of gravity relative to the chip surface. However, the value of q_{CHF} is much smaller for the vertically mounted chip. Honda et al. [7] have shown that this difference is closely related to the difference in the residence time of large secondary bubbles on the chip surface between the two cases. It is relevant to note here that the other micro-pin-finned chips showed the heat transfer characteristics similar to the case of chip PF50-200. For chip S, the value of q is much higher for the vertically mounted chip in the nucleate boiling region, which shows predominant effect of the direction of gravity relative to the chip surface. The q_{CHF} is somewhat smaller for the vertically mounted chip. The ratio of q_{CHF} for the vertically mounted and horizontally mounted chips is about 0.75 and 0.95 for chips PF50-200 and S, respectively. The q_{CHF} ratio for all micro-pin-finned chips ranged from 0.75 to 0.91. These values agree fairly well with 0.86 obtained from the empirical equation for the heater orientation effect on q_{CHF} proposed by Chang and You [21].

Fig. 8 compares the boiling curves for all chips at $\Delta T_{sub} = 0$ K (degassed FC-72). All chips follow almost the same q versus ΔT_{sat} relation in the non-boiling region. This indicates that the inter-fin spacing of micro-pin-fins ($= 30$ or 50 μm) is so small that the gap between adjacent fins is completely submerged in the layer of superheated liquid. The chain line in Fig. 8 shows the prediction of empirical equation for free convection heat transfer on an upward-facing horizontal surface proposed by Fishenden and Saunders [22]. The measured heat flux in the non-boiling region is about 130% higher than the predicted value. Sample calculation was made to estimate heat loss to bulk liquid by heat conduction through the Pyrex glass plate and the copper lead wires. By using the free convection heat transfer coefficient at $\Delta T_{sat} = 20$ K ($= 280$ W/m^{2}K) and the dimensions of glass plate and lead wires, the equivalent heat transfer area due to the fin effect is calculated to be 90.5 and 14.4 mm^2 for the glass plate and the lead wires, respectively. In addition, the side surface area of chip directly exposed to FC-72 is about 10 mm^2. Thus the sum of these heat transfer area is 114.9 mm^2. This indicates that the difference between the measured and calculated heat fluxes in the free convection region is due to additional heat transfer from these surfaces. The wall superheat at boiling incipience $\Delta T_{sat,i}$ is about 14.3, 15.5, 16.7, 20.4,

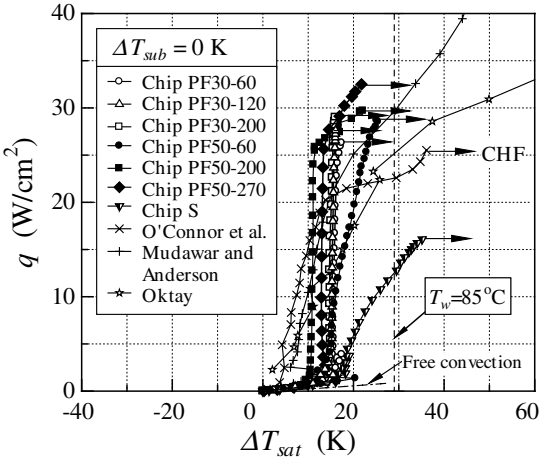


Fig. 8. Comparison of boiling curves; $\Delta T_{sub} = 0$ K, degassed.

12.8 and 13.3 K for chips PF30-60, PF30-120, PF30-200, PF50-60, PF50-200 and PF50-270, respectively. The temperature overshoot (decrease in wall temperature at boiling incipience) ranges from 1.0 to 10.0 K depending on the chip. All the micro-pin-finned chips show considerable heat transfer enhancement in the nucleate boiling region as compared to chip S. It is seen that chips PF30-60, PF30-120 and PF30-200 show almost the same boiling curve (except for the region near the CHF point) with a very steep increase in q with increasing ΔT_{sat}. Chips PF50-200 and PF50-270 also show a very steep increase in q with increasing ΔT_{sat}. However, the boiling curves of these chips show a bend at $q \approx 26$ W/cm^2 and the slope decreases severely at higher q. This is probably due to the partial dryout of the gap between adjacent fins. The boiling curve of chip PF50-60 shows a larger ΔT_{sat} and smaller slope than the other micro-pin-finned chips. Comparison of chips PF50-60, PF50-200 and PF50-270 reveals that the boiling curve shifts toward a smaller ΔT_{sat} in the order of chips PF50-60, PF50-270 and PF50-200 in the region of $q < 26$ W/cm^2. This order is in accord with the increase of surface roughness on the fin flank observed in Fig. 3. For all the micro-pin-finned chips, the value of q_{CHF} is much higher than that for chip S and the value of T_w at the CHF point is smaller than the maximum allowable temperature for LSI chips ($= 85$ °C). In Fig. 8, the boiling curves for the enhanced surfaces with about 1-mm-high dendritic structure obtained by Oktay [1], micro-pin-fins with the dimensions of $0.305 \times 0.305 \times 0.508$ mm^3 and the fin spacing of 0.305 mm by Mudawar and Anderson [14], and a porous layer consisting of 8–12 μm diamond particles by O'Connor et al. [19] are also shown for comparison. For these surfaces, the slope of boiling curve decreases as ΔT_{sat} increases and the wall temperature at the CHF point is greater than 85 °C. While the values of q_{CHF} for Oktay [1] and Mudawar and Anderson [14] are greater than those for the micro-pin-finned chips, the maximum allowable heat fluxes q_{max} (i.e., value of q at $T_w = 85$ °C) are comparable to q_{CHF} for the latter.

Fig. 9 compares the boiling curves for all chips immersed in degassed FC-72 at $\Delta T_{sub} = 25$ K. In Fig. 9, the prediction of free convection correlation [22] is also shown by a chain line. Again, the measured heat flux in the non-boiling region is 100–130% higher than the prediction. The trend of experimental data is basically the same as the case of $\Delta T_{sub} = 0$ K shown in Fig. 8 except that the values of $\Delta T_{sat,i}$ and the temperature overshoot are somewhat higher and the critical heat flux increases considerably. It is relevant to note here that chip PF50-60 shows a peculiar boiling curve in the low heat flux region of nucleate boiling. The value of ΔT_{sat} first increases as q increases. Then ΔT_{sat} decreases, and then it increases again, with further increasing q.

Fig. 10 compares the boiling curves for all chips immersed in gas-dissolved FC-72 at $\Delta T_{sub} = 25$ K. In this case bubble generation occurs at a smaller ΔT_{sat} ($= 7.1$–15.8 K). As a result, heat transfer in the low ΔT_{sat} region is enhanced as compared to the degassed FC-72 shown in Fig. 9. Even in this case the temperature overshoot is observed for a number of chips. The heat transfer characteristics in the nucleate boiling region and the value of q_{CHF} are close to the case of degassed FC-72.

Figs. 11 and 12, respectively, compare the boiling curves for all chips immersed in degassed and gas-dissolved FC-72 at $\Delta T_{sub} = 45$ K. As expected, the heat transfer characteristics are similar to the corresponding cases at $\Delta T_{sub} = 25$ K shown in Figs. 9 and 10 except that the value of $\Delta T_{sat,i}$ for gas-dissolved FC-72 is smaller and q_{CHF} increases significantly. The highest

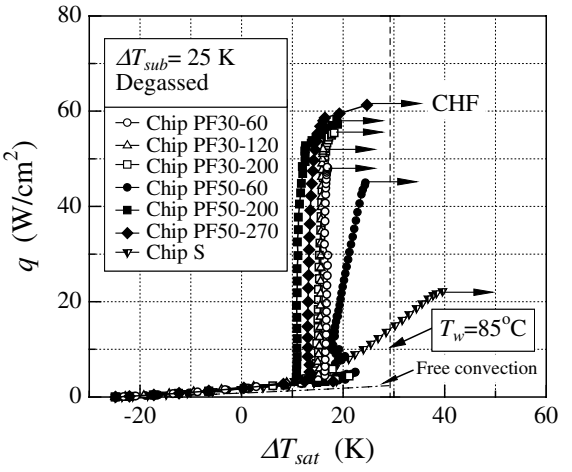


Fig. 9. Comparison of boiling curves; $\Delta T_{sub} = 25$ K, degassed.

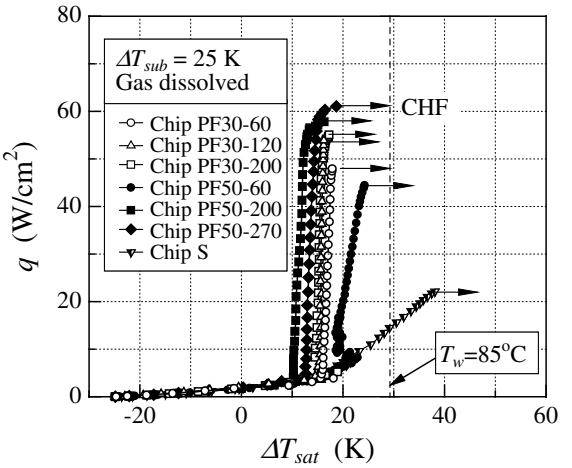


Fig. 10. Comparison of boiling curves; $\Delta T_{sub} = 25$ K, gas-dissolved.

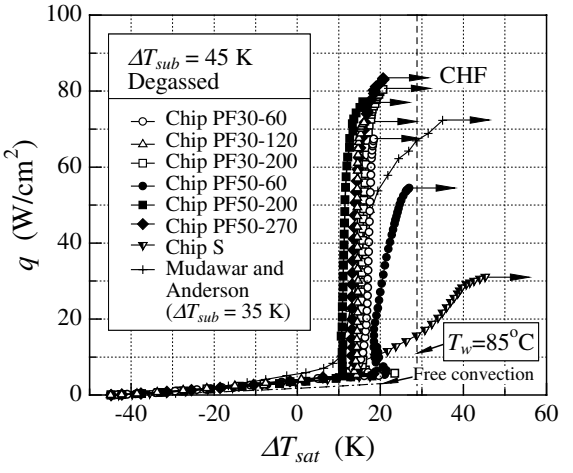


Fig. 11. Comparison of boiling curves; $\Delta T_{sub} = 45$ K, degassed.

value of q_{CHF} ($= 84.5$ W/cm^2), about 2.9 times as large as that for a smooth surface, was obtained by chip PF50-270 with gas-dissolved FC-72 (see Fig. 12). In Figs. 11 and 12, the results for micro-pin-finned surface by Mudawar and Anderson [14] and diamond-treated surface by O'Connort et al. [19] are respectively shown for comparison. It should be mentioned here that the value of ΔT_{sub} is smaller for these surfaces. As was the case of $\Delta T_{sub} = 0$ K shown in Fig. 8, the boiling curves of these surfaces show a smaller slope than the micro-pin-finned chips.

The micro-pin-finned chips tested in the present study are characterized by a very sharp increase in q with increasing ΔT_{sat}. As described previously, the boiling curve shifts toward a smaller ΔT_{sat} as the surface roughness on the fin flank increases. Considering these results and the behavior of growing bubbles shown in Figs. 4 and 5, the bubble nucleation is supposed to occur mainly at the fin flank. Since the micro-pin-fins are completely submerged in the layer of superheated liquid and the surface roughness is supposed to be almost uniform for all fins, the condition for bubble nucleation will be satisfied at almost the same ΔT_{sat} at all parts of the chip surface. Thus the boiling phenomena will not be affected by the fluid flow and heat transfer on the chip surface as long as the liquid supply to the gap between adjacent fins is not blocked by large secondary bubbles. As a result, the number of nucleation sites will increase very rapidly as ΔT_{sat} increases, resulting in a very steep boiling curve. For chip PF50-60 with the smallest fin height to fin pitch ratio, however, a peculiar boiling curve is observed in the low-heat-flux region of nucleate boiling and the slope of boiling curve in the fully developed nucleate boiling region is smaller than the other micro-pin-finned chips (see Figs. 8–12). These results indicate that the bubble nucleation on this chip was more or less affected by the local fluid flow and heat transfer on the chip surface. This is in accord with the fact that the bubble emission period on chip PF50-60 at low q was much longer than that for chip S but was shorter than that for chip PF50-200.

Fig. 13 shows q_{CHF} for all chips plotted as a function of the surface area enhancement ratio, A_t/A, with ΔT_{sub} as a parameter, where A_t is the surface area of top surface including the fin flank and fin root surfaces and A is the base surface area ($= 1$ cm^2). Since the values of q_{CHF} for degassed and gas-dissolved FC-72 are close to each other, only the results for degassed FC-72 are presented for clarity. For a fixed value of t ($= 30$ or 50 μm), q_{CHF} increases monotonically with increasing A_t/A (i.e., with increasing h). For all chips, q_{CHF} increases with increasing ΔT_{sub} and the effect of surface area enhancement is

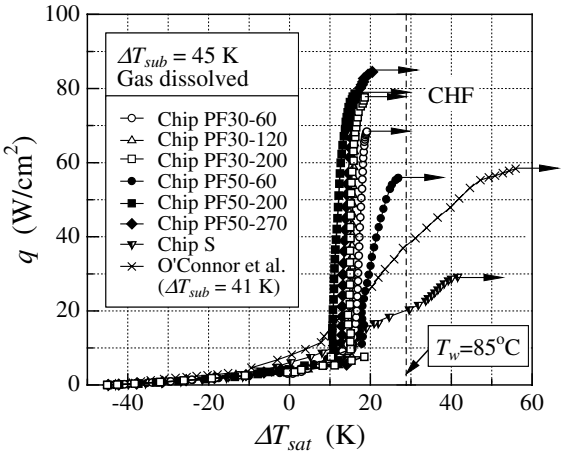


Fig. 12. Comparison of boiling curves; $\Delta T_{sub} = 45$ K, gas-dissolved.

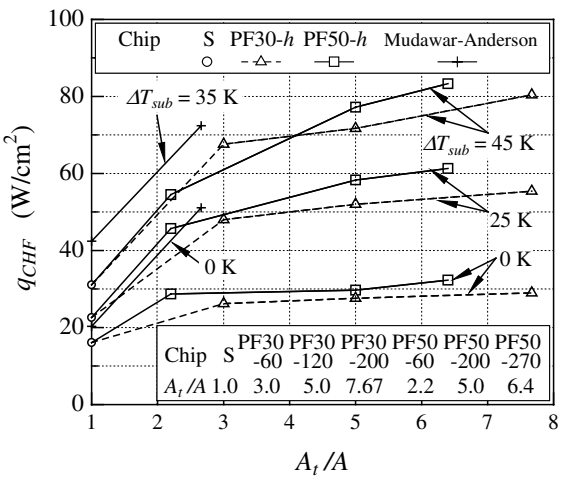


Fig. 13. Variation of q_{CHF} with A_t/A, degassed.

more significant for higher ΔT_{sub}. It is also seen that, for a fixed value of A_t/A, chips PF50-h with a larger t give a higher q_{CHF} than chips PF30-h. In Fig. 13, the results for the micro-pin-finned surface of Mudawar and Anderson [14] with a much larger fin size ($t = 305$ μm, $p = 610$ μm and $h = 508$ μm) are also shown for comparison. This surface shows a higher q_{CHF} than chips PF30-h and PF50-h at the same A_t/A. It should be mentioned here, however, that the wall temperature at the CHF point of Mudawar and Anderson [14] is greater than 85 °C (see Figs. 8 and 11). The above results are in contrast to the case of micro-pin-finned chips with constant h ($= 60$ μm) and variable t ($= 10$–50 μm) shown in Honda et al. [8], where q_{CHF} took the maximum values at $A_t/A = 2.2$ (i.e., $t = 50$ μm) for $\Delta T_{sub} = 0$ and 3 K, and at $A_t/A = 3.0$ (i.e., $t = 30$ mm) for $\Delta T_{sub} = 25$ and 45 K, respectively. These results indicate that q_{CHF} depends not only on A_t/A but also on the limitation of liquid supply to the gap between adjacent fins.

Fig. 14 shows the dimensionless quantity, $(q_{CHF}/q_{CHF,S})/(A_t/A)$, for all chips at $\Delta T_{sub} = 0$ and 45 K plotted as a function of A_t/A. If all part of the micro-pin-finned surface is equally effective for heat transfer at the CHF point, the value of $(q_{CHF}/q_{CHF,S})/(A_t/A)$ should be equal to unity irrespective of A_t/A. Actually, however, $(q_{CHF}/q_{CHF,S})/(A_t/A)$ decreases from unity as A_t/A increases. Comparison of chips PF30-h and PF50-h reveals that $(q_{CHF}/q_{CHF,S})/(A_t/A)$ at the same A_t/A is higher for chips PF50-h with larger fin size. In Fig. 14, the previous results for chips PFt-60 with constant h ($= 60$ μm) and variable t are also shown for comparison. The value of p is equal to $2t$ for all chips. For these chips A_t/A is larger for smaller t ($A_t/A = 4$ and 7 correspond to the cases of $t = 20$ and 10 μm, respectively). Generally, chips PFt-60 give a lower $(q_{CHF}/q_{CHF,S})/(A_t/A)$ than chips PF30-h and PF50-h for $A_t/A \geqslant 4$. This again indicates that a

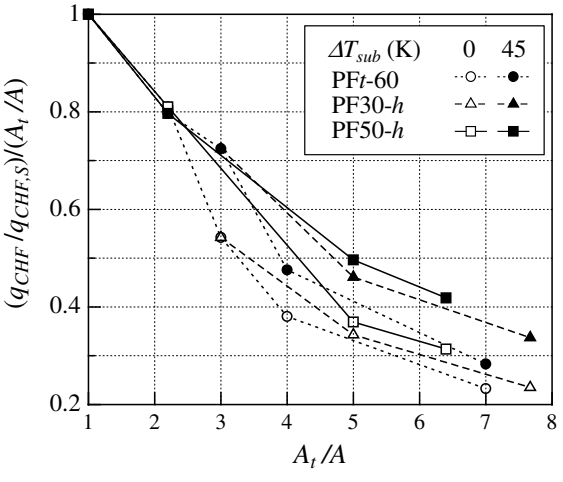


Fig. 14. Variation of $(q_{CHF}/q_{CHF,S})/(A_t/A)$ with A_t/A, degassed.

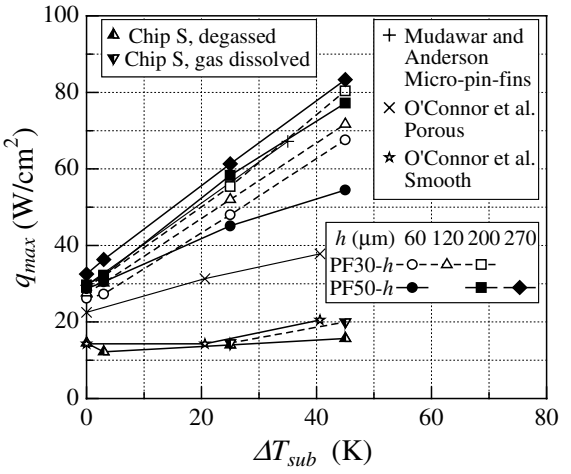


Fig. 15. Variation of q_{max} with ΔT_{sub}, degassed for chips PF30-h and PF50-h.

larger fin size is more effective in increasing q_{CHF}. It is also seen from Fig. 14 that $(q_{CHF}/q_{CHF,S})/(A_t/A)$ increases as ΔT_{sub} increases. The increase is more significant for larger A_t/A.

As stated previously, the upper limit of temperature for a reliable operation of LSI chips is given by 85 °C. Thus the maximum allowable heat flux q_{max} is given by q_{CHF} if $T_{w,CHF} < 85$ °C and by q at $T_w = 85$ °C if $T_{w,CHF} > 85$ °C. Fig. 15 shows q_{max} for chips S, PF30-h and PF50-h plotted as a function of ΔT_{sub}. In Fig. 15, only the results for degassed FC-72 are presented for clarity. The experimental data by Mudawar and Anderson [14] and O'Connor et al. [19] are also shown for comparison. The q_{max} of micro-pin-finned surface by Mudawar and Anderson [14] is close to those of the chips PF30-200 and PF50-200. The porous surface of O'Connor et al. [19] shows the q_{max} value in between those for the micro-pin-finned chips and the smooth chip. The highest q_{max} is obtained by chip PF50-270 with the largest fin size among the chips tested in the present study. The highest value of q_{max} ($= 84.5$ W/cm^2), 4.2 times as large as that for chip S, was obtained by the gas-dissolved FC-72 at $\Delta T_{sub} = 45$ K.

4. Conclusions

(1) The micro-pin-fins were effective in enhancing heat transfer in the nucleate boiling region and increasing q_{CHF}. The boiling curve of the micro-pin-finned chip was characterized by a very sharp increase in the heat flux with increasing wall superheat. The slope of boiling curve was somewhat smaller for chip PF50-60 with the smallest fin height to fin pitch ratio. The wall superheat in the fully developed nucleate boiling region was lower for chips with larger

surface roughness on the fin flank. For the chips with high fins ($\geqslant 200$ μm), however, the boiling curve showed a bend in the high-heat-flux region and the slope decreased significantly. The wall temperature at the CHF point was always less than the upper limit for a reliable operation of LSI chips ($=85$ °C).

(2) The gas-dissolved FC-72 showed a marked decrease in the boiling incipience temperature. As a result, the heat transfer performance in the low-heat-flux region was higher than that for the degassed FC-72. However, the heat transfer performance in the high-heat-flux region was close to each other.

(3) Comparison of horizontally mounted and vertically mounted micro-pin-finned chips revealed that while the heat transfer performance in the low-heat-flux region was higher for the vertically mounted chip, the boiling curve in the fully developed nucleate boiling region was close to each other and the critical heat flux was much lower for the vertically mounted chip. The ratio of q_{CHF} between the horizontally mounted and vertically mounted micro-pin-finned chips ranged from 0.75 to 0.91. This agreed fairly well with the prediction of empirical equation for the surface inclination effect proposed by Chang and You [21].

(4) For a fixed value of t ($=30$ or 50 μm), q_{CHF} increased monotonically with increasing h (i.e., increasing surface area enhancement ratio A_t/A) in the range of 60–270 μm. For a fixed value of A_t/A, q_{CHF} was higher for larger t. This was in contrast to the previous results for fixed h ($=60$ μm) and variable t ($=10$–50 μm) where q_{CHF} took a maximum value at $t = 50$ μm ($A_t/A = 2.2$) for $\Delta T_{sub} = 0$ and 3 K, and at $t = 30$ μm ($A_t/A = 3.0$) for $\Delta T_{sub} = 25$ and 45 K.

(5) The value of dimensionless quantity $(q_{CHF}/q_{CHF,S})/(A_t/A)$ decreased from unity as the A_t/A ratio increased. This indicated that the ratio of surface area effective for heat transfer at the CHF point decreased with increasing A_t/A. For a fixed value of A_t/A, $(q_{CHF}/q_{CHF,S})/(A_t/A)$ was higher for larger fin size and higher ΔT_{sub}.

(6) For all chips, the maximum allowable heat flux q_{max} (i.e., q_{CHF} for chips with $T_{w,CHF} < 85$ °C and q at $T_w = 85$ °C for chips with $T_{w,CHF} > 85$ °C) increased almost linearly with increasing ΔT_{sub}. The highest value of q_{max} ($=84.5$ W/cm^2), 4.2 times as large as that for chip S, was obtained by the combination of chip PF50-270 and gas-dissolved FC-72 at $\Delta T_{sub} =$ 45 K.

Acknowledgements

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